REMARKS

The Final Office Action mailed January 29, 2004, has been received and reviewed. Claims 1 through 9, and 12 through 19 are currently pending in the application. Claims 1 through 9, and 12 through 19 stand rejected Applicant proposes to amend claims 1 and 13, and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in view of U.S. Patent No. 5,909,559 to So

Claims 1 through 3, 5 through 7, 10 (Claim 10 was previously cancelled), and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-3, 5-7, 10 and 12 are improper because the elements for a *prima facie* case of obviousness are not met to establish a prima facie case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination

and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure, to establish a prima facie case of obviousness.

Generally

The Office Action alleges specific disclosures regarding the Dea reference which Applicants individually address hereinbelow, however, Applicants take issue herein with the Response to Arguments regarding Applicants' previous arguments.

In the Office Action's Response to Arguments, the Office Action states:

> So was cited only to suggest the conventional well-known North Bridge chip. Applicant do not credibly argue, nor could him, that it would have been unobvious to incorporate the well known North Bridge chip into Dea's system. The examiner believes that the artisan would have recognized the obviousness of the well-known North bridge chip of So and would have combined the references as proposed by the examiner. (Office Action p. 4, emphasis added).

Applicants acknowledge that conventional "North Bridge chips" are known in the art. However, Applicants' invention as claimed does not incorporate a **conventional** North Bridge chip into a video compression architecture. Furthermore, any proper combination of the Dea and So references could not teach or suggest Applicants' invention as claimed. Specifically, if the concept of a North Bridge were somehow incorporated within the Dea reference then it may find utility in providing a bridge between the processor and the system memory which would enable the processor to read and write data from and to the system memory without burdening the system bus. However, the compression/decompression accelerator 120 of Dea that the Examiner equates to Applicants' core logic chip, according to the architecture of Dea, would remain a peripheral device that interacts with a shared bus. There is no teaching or suggestion within either of the references or any combination thereof to further integrate separate functionality (e.g., differencing capability, dedicated video input) into an embodiment that utilizes a North Bridge architecture to facilitate improved interaction between the processor and system memory.

Furthermore, there is no teaching or suggestion to further integrate a specific dedicated video data interface into a North Bridge that has been previously integrated within the teachings

of Dea. The North Bridge of So does not contemplate additional dedicated interfaces such as Applicants' core logic chip with a dedicated video input, as claimed by Applicants. Therefore, Dea and So, either individually or in any proper combination, do not teach, suggest or motivate Applicants' invention as claimed.

Claim 1

Regarding amended independent claim 1, the Office Action alleges that:

> Considering claim 1 (Four Time Amended), Dea discloses a remote video processing system including compression/decompression accelerator. Dea discloses the following claimed subject matter, note:
>
> a) the claimed method for compressing video data in a computer system is met by the description at column 4, lines 36-41 and lines 17-19, and FIG. 1, where of the described compression /decompression accelerator 120 performs the compression method;
>
> b) the claimed step of receiving a current video frame at a core logic chip in the computer system from a video source originating the video frame is met by description at column 6, lines 42-44 and FIG. 2; (Office Action p. 5, emphasis added).

Applicants respectfully direct the Examiner's attention to FIG. 2 of Dea and note that FIG. 2 is a detailed diagram of Dea's compression/decompression accelerator 120 of Dea's FIG. 1 which illustrates the **indirect** coupling of the video source (camera) 127 through a **shared** bus 116, 118 to compression/decompression accelerator 120.

In distinct contrast, Applicants, in amended independent claim 1, specifically recite:

> receiving a current video frame at a **dedicated video input of a core logic chip** in the computer system **directly** from a video source originating the video frame, the computer system including the core logic chip for **directly** coupling a processor to a system memory and for coupling the processor and the system memory to a system bus . . .. (Applicants' Amended Independent Claim 1, emphasis added).

Because of the shared bus configuration of Dea, the available bandwidth for such an architecture is greatly curtailed due to the necessity of sharing the bus with data traffic destined

for other resources. It should be apparent that Dea does not teach, suggest or provide any motive for a dedicated video input of a core logic chip. Therefore, the rejection should be withdrawn.

The Office Action continues by further alleging that:

> c) the teaching of "the computer system including the core logic unit for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" which is described and depicted on Fig. 1 and column 4, lines 37-60, where as Fig. 1 depicts the compress/decompression accelerator 120 (core logic unit) is coupled to processor 112 and DRAM 114 (system memory) through the data and system bus 116, 118; (Office Action pp. 5-6, emphasis added).

Applicants respectfully direct the Examiner's attention to FIG. 1 of Dea and note that the processor 112 and memory 114 are **NOT** coupled through the compression/decompression accelerator 120 but are instead coupled through a bus 116, 118.

In distinct contrast, Applicants, in amended independent claim 1, specifically recite:

> receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including **the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus** . . .. (Applicants' Amended Independent Claim 1, emphasis added).

Because of the shared bus configuration of Dea, the processor 112 reads and writes data from and to the memory 114 independent of any influence or accommodation by compression/decompression accelerator 120. Additionally, the compression/decompression accelerator 120 of Dea does **NOT** couple the processor 112 and system memory 114 to the system bus 116, 118. Therefore, Dea does not teach, suggest or provide any motive for "core logic chip for directly coupling a processor to a system memory and for coupling the processor and system memory to a system bus" as claimed by Applicants. Therefore, the rejection should be withdrawn.

The Office Action continues by further alleging that:

> d) the claimed step of computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the core logic chip is met by the description of the subtraction function of frame difference block 220 column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2); (Office Action pp. 5-6, emphasis added).

Applicants respectfully reiterate that the compression/decompression accelerator 120, which the Office Action is equating to Applicants' core logic chip does **NOT** include a dedicated interface for directly receiving video data. Applicants further assert as illustrated in Dea's FIG. 1, the **indirect** coupling of the video source (camera) 127 through a **shared** bus 116, 118 to compression/decompression accelerator 120 rather than through a separate dedicated interface.

In distinct contrast, Applicants, in amended independent claim 1, specifically recite:

> **computing at the core logic chip a difference frame** from the current video frame and a previous video frame **as the current video frame streams into the dedicated video input of the core logic chip** the difference frame including computing the difference frame in the core logic chip within the computer system, wherein the core logic chip is a north bridge chip; . . .. (Applicants' Amended Independent Claim 1, emphasis added).

Dea teaches of the indirect coupling of the video source (camera) 127 through a shared bus 116, 118 to compression/decompression accelerator 120 rather than a dedicated video input of the core logic chip. Therefore, Dea does not teach, suggest or provide any motive for "computing at the core logic chip a difference frame . . . as the current video frame streams into the dedicated video input of the core logic chip" as claimed by Applicants. Therefore, the rejection should be withdrawn.

The Office Action continues by further alleging that:

> e) the claimed step of storing difference frame in the system memory into the computer system which is met by memory 114 as described at column 9, line

> 60 to column 10, line 3, column 11, lines 1-13 and FIG. 2, whereas the passage bridging from column 9 and 10 describes the frame difference encoding data by the encoder block 246 is first stored in the buffer 248, and the passage from column 11 further discloses the run/value pairs from the encoder 246 are applied to the encoded output circular buffer 332, in which the buffer 332 may located in DRAM memory 114 (Office Action p. 6, emphasis added).

Applicants respectfully reiterate that the processor 112 and memory 114 of Dea are **NOT** coupled through the compression/decompression accelerator 120 but are instead coupled through a bus 116, 118.

In distinct contrast, Applicants, in amended independent claim 1, specifically recite:

> storing the difference frame **directly from the core logic chip to the system memory** in the computer system **via a dedicated memory interface therebetween** . . .. (Applicants' Amended Independent Claim 1, emphasis added).

Because of the shared bus configuration of Dea, the processor 112 reads and writes data from and to the memory 114 independent of any influence or accommodation by compression/decompression accelerator 120. Additionally, the compression/decompression accelerator 120 of Dea does **NOT** couple the processor 112 and system memory 114 to the system bus 116, 118. Therefore, Dea does not teach, suggest or provide any motive for "storing the difference frame directly from the core logic chip to the system memory" as claimed by Applicants. Therefore, the rejection should be withdrawn.

The Office Action continues by further alleging that:

> f) the teaching of "the difference frame includes computing the difference frame in a core logic unit within the computer system" as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1, 2); and
>
> g) the teaching of "the processor retrieving the difference frame directly from the system memory via the core logic unit to complete compression of the

> video data which as describe at column 11, lines 19-33. (Office Action p. 6, emphasis added).

Applicants respectfully reiterate that the processor 112 and memory 114 of Dea are **NOT** coupled through the compression/decompression accelerator 120 but are instead coupled through a bus 116, 118.

In distinct contrast, Applicants, in amended independent claim 1, specifically recite:

> the **processor retrieving** the difference frame **directly from the system memory via the core logic chip using a dedicated processor interface therebetween** to complete compression of the video data. (Applicants' Amended Independent Claim 1, emphasis added).

Because of the shared bus configuration of Dea, the processor 112 reads and writes data from and to the memory 114 independent of any influence or accommodation by compression/decompression accelerator 120. Additionally, the compression/decompression accelerator 120 of Dea does **NOT** couple the processor 112 and system memory 114 to the system bus 116, 118. Therefore, Dea does not teach, suggest or provide any motive for "retrieving the difference frame directly from the system memory via the core logic chip" as claimed by Applicants. Therefore, the rejection should be withdrawn.

Claims 2-3, 5-7 and 12 (Claim 10 was previously cancelled)

Regarding claims 2-3, 5-7 and 12, while the Office Action cites further rejections, claims 2-3, 5-7 and 12 depend from amended independent claim 1 which is allowable in view of the preceding remarks. Therefore, for at least their dependency upon allowable claim 1, 2-3, 5-7 and 12 are allowable over the cited prior art and the respective rejections should be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea and U.S. Patent No. 5,909,559 to So, and further in view of U.S. Patent No. 4,546,383 to Abramatic et al.

Claims 4, 9, 13 through 17, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) and So (U.S. Patent No. 5,909,559), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claims 4, 9, 13 through 17 and 19

Claims 4, 9, 13 through 17 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) and So (U.S. Patent No. 5,909,559), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383).

The 35 U.S.C. § 103(a) obviousness rejections of claims 4, 9, 13-17, and 19 are improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding amended independent claim 13, Applicants claim:

> A method for compressing video data in a computer system comprising:
> **receiving a current video frame at a dedicated video input of a core logic chip** in the computer system **directly from a video source originating the video frame**, the computer system including **the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus**;
> computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into **the dedicated video input of** the core logic chip, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes **computing the difference frame in the core logic chip** within the computer system, wherein the core logic chip is a north bridge chip;
> storing the difference frame **directly from the core logic chip** into the system memory in the computer system **via a dedicated memory interface therebetween**;
> storing the current video frame **directly from the core logic chip** into the system memory in the computer system **using a dedicated processor interface**

therebetween;
the processor retrieving the difference frame directly from the system memory via the core logic chip; and
compressing the video data using the difference frame to produce compressed video data. (Emphasis added.)

Applicants reiterate the arguments presented above regarding the teachings and lack thereof regarding the previously discussed references. Specifically, Dea, So, and Abramatic do not appear to teach or suggest "**receiving a current video frame at a dedicated video input of a core logic chip . . . directly from a video source originating the video frame . . . the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame . . . as the current video frame streams into the dedicated video input of core logic chip** . . . the difference frame including **computing the difference frame in the core logic chip** . . .; **storing the difference frame directly from the core logic chip into the system memory in the computer system via a dedicated memory interface therebetween** . . .; and the **processor retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data**", as claimed by Applicants.

Generally, Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicant, by "receiving a current video frame at a dedicated video input of a core logic chip . . . directly from a video source originating the video frame . . . the core logic chip for directly coupling a

processor to a system memory and for coupling the processor and the system memory to a system bus" and "computing at the core logic chip the difference frame . . . as the current video frame streams into the dedicated video input of the core logic chip . . . the difference frame includes computing the difference frame in the core logic chip . . .".

Regarding So, while So gratuitously states that:

> In an architecture where no video is carried on the PCI bus, a VSP used as a graphic accelerator is still important because it is then advantageously provided either at the North Bridge or AGP graphics/video chip location so that advantageous MIPS are provided without substantially loading the PCI bus. (col. 17, lines 24-29)

So, like Dea, does not teach or suggest "receiving a current video frame at a dedicated video input of a core logic chip . . . directly from a video source originating the video frame . . . the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame . . . as the current video frame streams into the dedicated video input of core logic chip . . . the difference frame including computing the difference frame in the core logic chip . . .; storing the difference frame directly from the core logic chip into the system memory in the computer system via a dedicated memory interface therebetween . . .; and the processor retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data", as claimed by Applicants.

Applicants submit that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference under 35 U.S.C. § 103 would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants' disclosure. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper.

Applicants submit that since both references are drawn to bus interface and memory store specific disclosures, there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure.

Regarding Abramatic, the Office Action cites Abramatic alleging that "Abramatic et al. teaches that a form of image compression consists [in] detecting variations (difference) between one image and the next as describe at column 2, lines 53-56 [and that] Abramatic discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image a the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame." (See Office Action, p. 9.) While Abramatic may disclose calculating a difference frame through the use of an exclusive-OR function, neither Dea, So, nor Abramatic, either individually or in any proper combination, teach suggest or motivate each of the elements of Applicants' claim 13 as amended.

Applicants submit that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference and further in view of the Abramatic reference under 35 U.S.C. § 103 would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants' disclosure. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper. Specifically, any combination of the difference frame generating architecture of Dea, which is exclusively bus interface and memory dependent, as substituted in place of the VSP and North bridge combination of So, would inevitably result in a memory and bus interface combination since the VSP of So is a digital signal processor-core which pulls data, for example frame data, from a memory store over a bus interface.

Applicants submit that there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure. Therefore, Applicants respectfully request that the rejection to claim 13, be withdrawn.

Claims 14 through 17 depend from amended independent claim 13 and, for at least that reason, are allowable and the corresponding rejections should be withdrawn.

Claim 8

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea and U.S. Patent No. 5,909,559 to So, and further in view of U.S. Patent No. 5,926,223 Hardiman

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) and So (U.S. Patent No. 5,909,559), and further in view of Hardiman (U.S. Patent No. 5,926,223). Applicant respectfully traverses this rejection, as hereinafter set forth.

The 35 U.S.C. § 103(a) obviousness rejection of claim 8 is improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding claim 8, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claim in claim 8, including all of the claim limitations of the base claim, namely, "computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 8, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 8 be withdrawn.

Claim 18

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea, U.S. Patent No. 5,909,559 to So, and U.S. Patent No. 4,546,383 to Abramatic et al., and further in view of U.S. Patent No. 5,926,223 Hardiman

Claim 18 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559) and Abramatic et al. (U.S. Patent No. 4,546,383) as applied to claim 13 above, and further in view of Hardiman (U.S. Patent No. 5,926,223).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding claim 18, Dea, So, Abramatic, and Hardiman, either individually, or in any combination, do not teach, suggest, or provide any motive for Applicants' invention as claim in claim 18, including all of the claim limitations of the base claim, namely, "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 18, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 18 be withdrawn.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1 and 13 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. The support for the amendments to further define the scope of the invention, namely the amendments for dedicated interfaces, is found in the specification and is further found in the drawings, specifically with reference to Applicants' FIG. 2. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1-9 and 12-19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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